EXHIBIT P

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC. Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC. and SAMSUNG SEMICONDUCTOR, INC., Defendants.	Civil Case No. 2:21-cv-00463-JRG **JURY TRIAL DEMANDED**

DEFENDANTS' RESPONSIVE CLAIM CONSTRUCTION BRIEF

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INTRODUCTION

The parties' claim construction disputes are the result of Netlist's protracted prosecution strategy. By serially prosecuting its patents through years of litigation and challenges at the Patent Office, Netlist's asserted claims are fragmented and disjointed and require construction. To address this, Samsung's proposed constructions are rooted in the claim language and specifications. Netlist's proposed constructions seek to ignore the claims, the specification, and the prosecution history all to capture claim scope to which it is not entitled. Samsung requests that the Court construe the claims in a way that comports with the intrinsic record.

I. OVERVIEW OF THE TECHNOLOGY

The '918 and '054 patents relate to computer memory devices "that employ different types of memory devices such as combinations of Flash and random access memories." '918 patent at 1:65-2:2. While the patents admit that the use of Flash and DRAM on the same printed circuit board existed prior to the patents, the patents claim to disclose a specific type of memory, called Flash DRAM Hybrid DIMM ("FDHDIMM"), that uses a specific controller to allegedly increase read and write data throughput. *See* '918 patent at 2:56-64, 10:52-56.

The '060 and '160 patents relates to "systems and methods for reducing the load of drivers of memory packages included on the memory modules." '060 patent at 1:18-22; '160 patent at 1:20-24. Both relate to memory that have a plurality of so called "array dies," a "control die," and at least two die interconnects. *See* '060/'160 patents at Abstract.

The '506 and '339 patents both relate to memory modules with data buffers, which the '339 patent admits existed prior to the patents. *See* '506 patent at Abstract; '339 patent at Abstract; 1:18-2:22, 6:65-7:43. The '339 patent discloses specific configurations for actively driving data signals between a memory controller and selected memory. *See* '339 patent at Abstract, 1:18-2:22, 6:65-7:43. The '506 patent claims to disclose distributed data buffers that include delay

circuits to delay data signals by an amount determined based on at least one of the module control signals. *See* '506 patent at Abstract.

II. DISPUTED CLAIM TERMS

A. The '918 & '054 Patents

1. "dual buck converter" / "dual-buck converter"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
"buck converter with two outputs outputting two distinct regulated voltages"	Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, a buck converter with two regulated voltage outputs whose amplitude may be the same or different")

The term "dual buck converter" is used in the patents in relation to combining two buck converters to output two distinct regulated voltages, not simply two outputs. *See* '918 patent at claim 2 ("the first and third buck converters are further configured to operate as a ***dual buck converter***"). The claims recite distinct buck converters operating as a "dual buck converter" to output distinct regulated voltages, which is the required function of the dual buck converter defined in the specification.

The only discussion of "dual buck converter" in the specification describes it outputting two voltages with different voltage levels. '918 patent at 29:46-50; *see also id.* at Figure 16 (depicting voltage 1104 going to "Isol Dev" (isolation device) and voltage 1105 going to "FPGA"). The dual buck converter having distinct voltages—in order to perform its specific function—is illustrated in Figure 16 below (annotation added), which depicts a "dual buck converter" outputting two distinct regulated voltages 1104 and 1105:

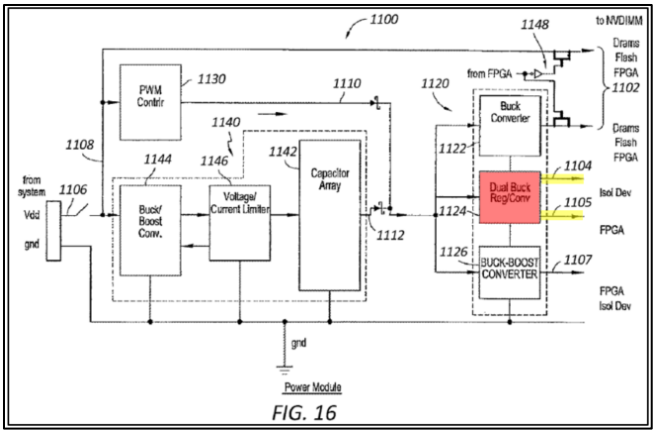


FIG. 16

This "dual buck converter" is defined as an element that provides different voltage values for different elements on the memory module. Here, the dual buck converter 1124 is part of the conversion element 1120, which serves to "provid[e] ***various voltage values*** to the memory system 1010." *Id.* at 29:18-27. The function of the conversion element 1120 is to reduce the voltage it receives to "an appropriate amount for powering various components of the memory system." *Id.* at 29:33-39. To this end, the dual buck converter "can provide the second voltage 1104 as well as another reduced voltage 1105." *Id.* at 29:44-46. It then must follow that the other reduced voltage 1105 would have a different voltage value than voltage 1104 because it is to be used by a different component of the memory system. The specification confirms this: "In one example embodiment, the second voltage 1104 is 2.5V and is used to power at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA)." *Id.* at 29:46-50. Samsung is thus not seeking to limit the patent to a single embodiment, as Netlist claims. Dkt. 76 at 24 (Netlist's Opening Brief) ("Netlist Br."). Rather, Samsung's construction gives "dual buck converter" the meaning it is given consistently throughout the claims and specification, including as part of the alleged invention. *See ICU Med., Inc. v. Alaris Med. Sys., Inc.*, 558 F.3d 1368, 1374-76 (Fed. Cir. 2009) (construing "spike" as requiring "an elongated structure having a pointed tip for piercing the seal"); *Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d

1313, 1319 (Fed. Cir. 2005) ("[i]t is [] entirely proper to consider the functions of an invention in seeking to determine the meaning of particular claim language"); *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1271 (Fed. Cir. 2001) ("[W]hen a patentee uses a claim term throughout the entire patent specification, in a manner consistent with only a single meaning, he has defined that term 'by implication.'").

Netlist has pointed to no part of the specification where the two voltages can be identical. The "alternative embodiments" do not concern the dual buck converter and do not establish that the dual buck converter can output two voltages with the same voltage level. '918 patent at 29:55-61. Rather, that part of the specification explains that the conversion element 1120 can have ***other*** sub-blocks that may produce different voltage values. *Id.*

2. "pre-regulated input voltage" / "input voltage"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
"regulated voltage generated on the memory module from an input voltage"	Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, modulated input voltage) / (that is, voltage that is provided to the earlier mentioned converters or converter circuit).

Because the '918 patent claims require both "a pre-regulated input voltage" and "an input voltage," they are presumed to have different meanings. *See CAE Screenplates Inc. v. Heinrich Fiedler GmbH & Co. KG*, 224 F.3d 1308, 1317 (Fed. Cir. 2000) ("In the absence of any evidence to the contrary, we must presume that the use of these different terms in the claims connotes different meanings."). Indeed, Netlist concedes that the two terms must have different meanings. *See* Netlist Br. at 25, n.14. The parties' dispute does not lie with "input voltage," but it is identified here for differentiation purposes. Instead, the parties' dispute lies with "pre-regulated" and specifically where the "pre-regulation" occurs.

The '918 patent claims make clear the "pre-regulation" occurs on the memory module itself. Asserted claim 16 requires that the voltage monitor circuit on the same memory module receive an input voltage from the module's edge connections: "a voltage monitor circuit configured to monitor ***an input voltage received via a first portion of the plurality of edge connections***." '918 patent at claim 16 (emphasis added). The claim also requires that the buck converters on the memory module receive a "pre-regulated input voltage: "first, second, and third buck converters configured to ***receive a pre-regulated input voltage*** and to produce first, second and third regulated voltages, respectively." *Id*. (emphasis added). Thus, the memory module generates the "pre-regulated input voltage" by receiving an "input voltage" and the generated "pre-regulated input voltage" is an input into the module's buck converters.

Additionally, the '918 patent specification unequivocally shows that the pre-regulation occurs on the memory module itself. Figure 16 of the '918 patent below shows the power module on the memory module (labeled 1100) (annotation added):

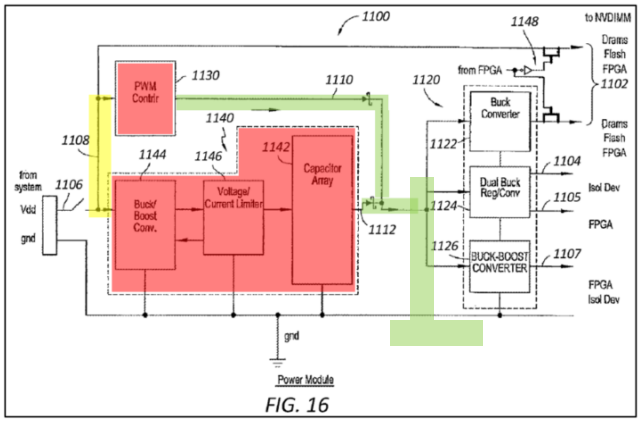


FIG. 16

As the '918 patent states, "[t]he power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems 1030, 1040." '918 patent at 28:3-5. The input voltage 1108 (yellow) is provided to the power module. *See id.* at 28:7-9 ("The power module 1100 comprises an input 1106 providing a third voltage 1108 to the power

module 1100 . . . ."). Power elements 1130 and 1140 (red) receive the input voltage and output a different voltage. *See id.* at 28:15-19 ("For example, in one example embodiment, the first power element 1130 is configured to receive a 1.8V input system voltage as the third voltage 1108 and to output a modulated 5V output as the fourth voltage 1110."); *see also id.* at 28:20-22.

The '918 patent makes clear that output voltages 1110, 1112 (green) from power elements 1130, 1140 are no longer "input voltages," but instead "pre-regulated input voltages":

> In addition, switching the point of power transition to be between the conversion element 1120 and the first and second power elements 1130, 1140 (***e.g., the sources of the pre-regulated fourth voltage 1110*** in the second state ***and the pre-regulated fifth voltage 1112*** in the third state) can smooth out potential voltage spikes.

'918 patent at 28:53-58 (emphasis added). Aside from the Abstract, this is the only mention of "pre-regulated" voltage in the '918 patent specification. In short, the power module on the memory module creates the "pre-regulated input voltage" and the term should be construed accordingly.

Netlist's proposed construction of "modulated input voltage" does not address the key dispute – where the "pre-regulated input voltage" is generated. Netlist argues that because power supply 1080 from a different embodiment "may not be on the same printed circuit board," its nebulous construction is correct. But this argument falls flat because the large swathes of specification (Netlist Br. at 26) it cites to link power supply 1080 in Figure 12 to power element 1140 in Figure 16 fail to mention power supply 1080. As such, this term should be construed consistent with the only disclosure of "pre-regulated" voltages in the specification, as "regulated voltage generated on the memory module from an input voltage."

3. "first" / "second" / "third" / "fourth" "regulated voltages" / first"; "second" / "third" / "fourth" "voltage amplitude"

"first" / "second" / "third" / "fourth" "regulated voltages"	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"first regulated voltage that is distinct from the second, third, and fourth regulated voltages" / "second regulated voltage that is distinct from the first, third, and fourth	"Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is,

regulated voltages" / "third regulated voltage that is distinct from the first, second, and fourth regulated voltages" / "fourth regulated voltage that is distinct from the first, second, and third regulated voltages"	first, second, third and fourth voltages that are adjusted, within tolerance, to a particular voltage level)."
"first" / "second" / "third" / "fourth" "voltage amplitude"	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"first voltage amplitude that is distinct from the second, third, and fourth voltage amplitudes" / "second voltage amplitude that is distinct from the first, third, and fourth voltage amplitudes" / "third voltage amplitude that is distinct from the first, second, and fourth voltage amplitude" / "fourth voltage amplitude that is distinct from the first, second, and third voltage amplitude"	"Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, first/second/third/fourth amplitude of voltage which nee not all be different)."

The use of "first," "second," "third," and "fourth" in the '918 patent claims is "a common patent-law convention to distinguish between repeated instances of an element." *3M Innovative Props. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1371 (Fed. Cir. 2003). "Where a claim lists elements separately, the clear implication of the claim language is that those elements are distinct components of the patented invention." *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010) (internal citations, quotations omitted).

Consistent with this Court's precedent, the enumerated "first," "second," "third," and "fourth" "regulated voltages" and "voltage amplitudes" should be construed as ***distinct*** elements that cannot be ***identical***. *See Alexsam, Inc. v. Cigna Corp.*, No. 2:20-cv-00081-JRG-RSP, 2021 WL 1561606, at *30 (E.D. Tex. Apr. 20, 2021) (construing "first database" as "a database that is ***distinct*** from the second database" and "second database" as "a database that is ***distinct*** from the first database" and noting "any dispute regarding 'distinct' relates to factual issues of infringement rather than any legal question for claim construction") (emphasis added); *Cioffi v. Google Inc.*, No. 2:13-cv-00103-JRG-RSP, 2014 WL 4293978, at *13-15 (E.D. Tex. Aug. 28, 2014) (construing "first memory space" as "memory space ***distinct*** from a second memory space" and "second memory space" as "memory space ***distinct*** from a first memory space") (emphasis added);

Mobile Telecomms. Techs., LLC v. Leap Wireless Int'l, Inc., No. 2:13-cv-00885-JRG-RSP, 2015 WL 2250056, at *7-9 (E.D. Tex. May 13, 2015) (finding that "[c]onstruction is appropriate to clarify that the 'first' and 'second' zones are not ***identical*** regions of space" and construing "second zone" as "portion of a region of space that is not ***identical*** to the 'first zone'") (emphasis added); *United Servs. Auto. Ass'n v. PNC Bank N.A.*, No. 2:20-cv-00319-JRG, 2021 WL 5451020, at *15 (E.D. Tex. Nov. 22, 2021) ("the 'first' and 'second' processing circuitry must be ***distinct*** from one another") (emphasis added).

The claims of the '918 patent make clear that the enumerated "regulated voltages" and "voltage amplitudes" are distinct. Asserted claim 1 recites discrete connections of the "first regulated voltage" to the "plurality of [SDRAM] devices," and of "both the second regulated voltage and the fourth regulated voltage" to "the at least one circuit." Similarly, dependent claims 3 and 4 of the '918 patent recite distinct voltage amplitudes for the enumerated "voltage amplitude**s**." '918 patent at claim 3 ("the first voltage amplitude is 1.8 volts"), claim 4 ("the second, third, and fourth voltage amplitudes are 2.5 volts, 1.2 volts, and 3.3 volts, respectively").

Indeed, Netlist fails to identify any claims that support a construction in which the "first," "second," "third," and "fourth" "regulated voltages" and "voltage amplitudes" can be identical.[1] Netlist identifies several claims that it purports are inconsistent with Defendants proposed construction, but those claims in fact demonstrate that the various "regulated voltages" and "voltage amplitudes" are distinct from one another. Netlist Br. at 20. Claim 1 of the '918 patent,

[1] Netlist is wrong to accuse Samsung's construction of "read[ing the] voltage amplitude limitation into the claims" that recite only "regulated voltages." Netlist Br. at 19-20. Indeed, the phrase "voltage amplitude" does not appear in Defendants' proposed construction for the "regulated voltage" terms. Netlist's reference to Samsung's IPR petitions is inapposite, as the petitions clearly assert that "no express constructions are needed for this proceeding." *See, e.g.*, Ex. A at 8 (IPR2022-00999, Paper 1 (Petition)).

for instance, specifies in the last limitation relative magnitudes of the "second voltage amplitude" output by the second buck converter" and the "fourth voltage amplitude" output by the converter circuit. Netlist Br. at 20; *see also* '054 patent at claim 2 (adding a similar limitation in a dependent claim). That element serves only to limit ***how*** those two amplitudes must be distinct. It does not otherwise supplant the claim language distinguishing the "first," "second," "third," and "fourth" "voltage amplitudes." And claim 29 of the '918 patent merely requires that the claimed SDRAM devices receive "at least one" of the enumerated "regulated voltages" that has an amplitude of 1.8V. It does not, as Netlist suggests, permit all of the "regulated voltages" to be identical.

Netlist's other arguments are equally unavailing. Defendants' construction does not require a finding of disavowal—only that the claims be construed consistent with the specification and the well-established body of patent law holding that separately-listed claim elements must be "distinct." *See* '918 patent at Figure 16 (identifying distinct voltage outputs 1102, 1104, 1105, 1107). Netlist points to an embodiment in which "volatile memory 1032 and nonvolatile memory 1042 are both powered by a 1.8V first voltage 1102." Netlist Br. at 21. But the "first voltage 1102" is a single voltage, even if provided to both volatile and nonvolatile memories. The other voltages output by the power module 1100 are still distinct: the "voltage 1104 is 2.5V," the "voltage 1105 is 1.2V," and the "voltage 1107 may be 3.3V." '918 patent at 29:44-54. In every instance, components requiring the same voltage receive a single voltage from a single output, and components requiring different voltages receive them from different voltage outputs. *Id*. at 28:13-19; 29:44-54; 29:58-61. Netlist's other citations similarly describe distinct input/output voltages and voltage outputs having "different voltage values." *Id*. Netlist's characterization (at 22) of its arguments during prosecution of related patents—including that "first and second volatile memories should not be the ***same*** DRAM" and that "the prior art did not ***distinguish*** between . . .

the first and second commands"—is also consistent with Defendants' construction.

On the other hand, Netlist's proposed constructions lack any support in the claims, the intrinsic record, or the law. With respect to the "regulated voltage" terms, Netlist's construction focuses on the meaning of "regulated" that is not at issue between the parties, and in any event, seeks to define that term as "adjusted, within tolerance, to a particular [level]" based on a series of dictionaries that carry little weight. *See United Servs.*, 2021 WL 5451020, at *5 ("*Phillips* rejected any claim construction approach that sacrificed the intrinsic record in favor of extrinsic evidence, such as dictionary definitions or expert testimony."). Netlist's attempt to insert a negative limitation into the construction of the "voltage amplitudes" terms is similarly without foundation. *See, e.g., Vertical Comp. Sys., Inc. v. Interwoven, Inc.*, No. 2:10-cv-00490-JRG, 2013 WL 5202685, at *9 (E.D. Tex. Sep. 16, 2013). Consistent with this Court's lengthy precedent, "first," "second," "third," and "fourth" should be construed to be distinct.

4. "at least three regulated voltages" / "plurality of regulated voltages"

"at least three regulated voltages"	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"at least three distinct regulated voltages"	"Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, three or more regulated voltages)."
"plurality of regulated voltages"	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"plurality of regulated voltages"	"Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, multiple regulated voltages)."

For the same reasons provided immediately above, Defendants' proposed constructions of the terms "at least three regulated voltages" and "plurality of regulated voltages" recited by the asserted independent claims of the '054 patent require that the "regulated voltages" be ***distinct*** from one another. The claims of the '054 patent make this clear.

With respect to "at least three regulated voltages" in asserted claim 1, the same claim is explicit that the "at least three regulated voltages" includes distinct "first and second regulated voltages," requiring a distinct "third regulated voltage" that is addressed in dependent claim 3. That claim 1 of the '054 patent groups the "first," "second," and "third" "regulated voltages" as "at least three regulated voltages" does not alter the fact that the regulated voltages are distinct from one another in the claims as well as the specification. *See, e.g.*, '054 patent at claim 2 (further specifying the respective amplitudes of the "first" and "second" "regulated voltages" of claim 1), Figure 16 (identifying distinct regulated voltage outputs 1102, 1104, 1105, 1107 from the buck converters of "conversion element 1120"). Similarly, claims 16 and 24 of the '054 patent require "a first regulated voltage of the plurality of regulated voltages" that is coupled to "the plurality of SDRAM devices," distinguishing that voltage from second and third "regulated voltages." That those claims further require "three buck converters, each of which is configured to produce a regulated voltage of the plurality of regulated voltages," further confirms that the "plurality of regulated voltages" cannot be identical. For these reasons and those stated above with respect to the "first," "second," "third," and "fourth" terms of the '918 patent, the '054 patent claims should be construed to require a distinct set of "at least three regulated voltages" (claim 1) and "plurality of regulated voltages" (claims 16, 24).

5. "a second plurality of address and control signals"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
"a second plurality of address and control signals that are distinct from a first plurality of address and control signals"	"Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, a second set of address and control signals)."

As explained with respect to the "first," "second," "third," and "fourth" terms above, Samsung's proposed construction serves to clarify that the "first" and "second" "pluralit[ies] of

address and control signals" must be ***distinct*** from one another. This construction is consistent with the "common patent-law convention" of using "'first' and 'second' . . . to distinguish between repeated instances of an element" frequently endorsed by this Court. *3M*, 350 F.3d at 1371.

Defendants' construction is supported by the asserted claims of the '918 patent that also distinguish between the "first" and "second" pluralities of address and control signals: the "first plurality of address of address and control signals" is received by the claimed "at least one circuit," while the "second plurality of address and control signals" is "output" by the "at least one circuit." '918 patent at claim 1. But Netlist's assertion that "the claim . . . does not preclude the input and output signals be wholly or partially the same" demonstrates why construction is nevertheless necessary here. Netlist Br. at 23. If the signals received and output by the "at least one circuit" were "wholly" the same, the patentee would have had no reason to draft the claims to specify "first" and "second." The case law commands the same result. *See Mobile Telecomms. Techs.*, 2015 WL 2250056, at *7 ("the 'first' and 'second' sets must be distinct in order to give meaning to all of the words of the claim") (citing *Merck & Co., Inc. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so."")). Netlist's proposed construction strips "first" and "second" of any meaning within the claims and seeks only to rewrite the claims to replace the word "plurality" with the word "set" without explanation. *See* Netlist Br. at 22-23. If such signals are not distinct form one another, they are not a "plurality" and replacing that word with "set" introduces ambiguity undermining the "more than one" aspect of the plain meaning of "plurality."

6. "A memory module"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
Preamble is non-limiting	Preamble is limiting

Netlist argues the preamble is limiting because it provides antecedent basis, but "whether to treat a preamble as a claim limitation is determined on the facts of each case in light of the claim as a whole and the invention described in the patent." *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 952 (Fed. Cir. 2006). Here, each of the bodies of the claims at issue, however, recites a structurally complete invention, and as a result, the preambles are non-limiting statements of intended purpose. *See Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (internal citations, quotations omitted). As claimed in exemplary claim 1 of the '054 patent, the claims requires a "printed circuit board (PCB)" configured a certain way, "a voltage conversion circuit coupled to the PCB" configured a certain way, and "a plurality of components coupled to the PCB" coupled a certain way. Because the claims at issue expressly recite this essence in their bodies, *see* '054 patent at 3:46-52, reference to their preambles (even with an antecedent basis) is not necessary for a proper understanding of the claimed invention. Thus, the presumption against finding the preamble limiting is not overcome. *See Sol IP, LLC v. AT&T Mobility LLC*, No. 2:18-CV-00526-RWS-RSP, 2019 WL 6878836, at *6 (E.D. Tex. Dec. 16, 2019) (finding preambles not limiting even though providing antecedent basis because "the preambles do not further define the 'wireless communication system,' and the 'performing cell search' language in the preambles is merely 'descriptive' of the limitations set forth in the body of the claim").

B. The '060 & '160 Patents

1. "array die"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
"array die that is different from a DRAM circuit"	Plain and ordinary meaning (that is, a die including memory cells)

Netlist is prevented from including DRAM circuits as part of its alleged invention, which it disclaimed to secure allowance. "An applicant's statements to the PTO characterizing its invention may give rise to prosecution disclaimer." *Tech. Props. Ltd. LLC v. Huawei Techs. Co.*,

849 F.3d 1349, 1357 (Fed. Cir. 2017). Such a disclaimer occurs if it is "clear and unmistakable to one of ordinary skill in the art." *Id.*; *see also id.* at 1359 ("The question is what a person of ordinary skill would understand the patentee to have disclaimed during prosecution . . . ."); *Omega Eng'g, Inc, v. Raytek Corp.*, 334 F.3d 1314, 1325-26 (Fed. Cir. 2003). "[P]rosecution disclaimer promotes the public notice function of the intrinsic evidence and protects the public's reliance on definitive statements made during prosecution." *Omega*, 334 F.3d at 1324.

During prosecution, the examiner rejected pending claim 1 (among other claims) based on prior art reference Rajan. *See* Ex. B at 4-9 (2013-10-11 Non-Final Office Action). The applicant argued Rajan's DRAM circuits are "different from array dies" recited in claim 1. *See* Ex. C at 10 (2014-01-14 Amendment) ("Rajan merely stacks DRAM circuits 206A-D, which are different from array dies . . . ."). The applicant's argument was a clear and unmistakable disclaimer assertion that an array die does not include DRAM circuits. *Tech. Props.*, 849 F.3d at 1359.

Netlist contends (at 28) that the applicant's argument on array dies should be considered part of the argument that ***Rajan's buffer die*** operates differently from the control die. But Netlist does not explain why the applicant's statement was necessary to that argument, and the Federal Circuit has "made clear [that] an applicant's argument that a prior art reference is distinguishable on a particular ground can serve as a disclaimer of claim scope even if the applicant distinguishes the reference on other grounds as well." *Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1374 (Fed. Cir. 2007). The applicant's argument about the control die does not negate the applicant's plain-English statement that array dies are "different from" DRAM circuits.

Indeed, if the applicant only intended to distinguish Rajan on the ground that the claimed control die operates differently than Rajan's buffer die, he could have done so without stating that ***DRAM circuits are different from array dies***. Netlist does not argue to the contrary. Because the

applicant argued that an array die is different than DRAM circuits, the public is entitled to rely on his characterization of the invention, even if he could have distinguished Rajan on a narrower basis, such as the control die alone. *Tech. Props.*, 849 F.3d at 1359 ("[T]he scope of surrender is not limited to what is absolutely necessary to avoid a prior art reference; patentees may surrender more than necessary."); *see also Uship Intell. Props., LLC v. United States*, 714 F.3d 1311, 1315 (Fed. Cir. 2013) ("The fact that the applicant may have given up more than was necessary does not render the disclaimer ambiguous.").

Claim 29 of the '060 patent does not negate the applicant's statement that Rajan's DRAM circuits are different from array dies. *See* Netlist Br. 28. Claim 29 recites that "each DRAM package compris[es] . . . array dies." Netlist does not explain how claim 29's reference to a "DRAM ***package***" means that array dies are identical with DRAM circuits. Netlist's reliance on *In re Varma*, 816 F.3d 1352, 1363 (Fed. Cir. 2016), is also off-point, because Netlist does not show how construing "array dies" consistent with the applicant's characterization would require the same phrase to be construed differently in differently claims.

Netlist's final attempt is to limit the applicant's disclaimer to how the Rajan's DRAM circuits are "stacked." This too lacks support. Although the applicant's remarks reference the stacking, *see* Ex. C at 10-11 (2014-01-14 Amendment), Netlist points to nothing that limits the applicant's array die argument to how the DRAM circuits are stacked. Netlist's argument is a *post hoc* attempt to create ambiguity where none exists. *Fantasy Sports Properties, Inc. v. Sportsline.com, Inc.*, 287 F.3d 1108, 1115 (Fed. Cir. 2002) ("[The patentee] cannot now be heard to argue *post hoc* that it was the combination of the aforementioned limitations that rendered its invention patentable over the prior art."); *Uship*, 714 F.3d at 1315 (giving up more than necessary

"does not render the disclaimer ambiguous"); *Tech. Props.*, 849 F.3d at 1359 ("Had those same arguments been made to the Patent Office, our construction may have been different . . . .").

Genuine Enabling and *Technology Properties* are inapposite. In *Genuine Enabling Tech. LLC v. Nintendo Co.*, the parties disagreed only on the boundary of the disclaimer—whether it should exclude signals below about 20 Hz (i.e., below the audio frequency spectrum), or signals below 500 Hz. 29 F.4th 1365, 1374-75 (Fed. Cir. 2022). The court tailored the disclaimer to the applicant's specific statements and found that any other boundary was not clearly supported. *Id.* at 1374 ("[T]he only disavowal of claim scope that is clear and unmistakable in the record before us is Mr. Nguyen's disavowal of signals below the audio frequency spectrum."). Samsung's proposed construction is in accord, because it ***mirrors the language of the applicant himself***, and Netlist does not show that the applicant clearly drew any different boundary. *Technology Properties* also supports Samsung's position, because there the court found a disclaimer in line with the applicant's own clear statements during prosecution even though a narrower disclaimer might have been possible. 849 F.3d at 1359. As in both of those cases, this Court should construe "array die" as consistent with the clear language of the applicant: "different from a DRAM circuit." Ex. C at 10 (2014-01-14 Amendment).

2. "chip select signal" / "chip select conduit"

Term	Defendants' Proposed Construction	Plaintiff's Proposed Construction
"chip select signal"	Plain and ordinary meaning	"signal for enabling or selecting one or more array dies for data transfer"
"chip select conduit"	Plain and ordinary meaning	"conduits for transmitting" "chip select signals," as construed above

Netlist seeks to rewrite the claim and ignore the word "select" under the guise of claim construction. It does so by expanding the coverage to a situation in which a chip select signal could enable multiple and even all array dies at once. But this is no selection at all and Netlist

points to nothing in the specification to support that view. *See* Netlist Br. at 30; *Nystrom v. TREX Co.*, 424 F.3d 1136, 1144–45 (Fed. Cir. 2005) ("Nystrom is not entitled to a claim construction divorced from the context of the written description . . . ."); *see also Nat'l Recovery Techs., Inc. v. Magnetic Separation Sys., Inc.*, 166 F.3d 1190, 1195 (Fed. Cir. 1999) ("The plain meaning of the term 'select,' including the dictionary meaning agreed upon by the parties, implies that some signals are to be picked or chosen and others are to be excluded based upon some special, unique or discrete quality."); *see also* Ex. D at 62 (Dictionary of Computing, A&C Black, Sixth Edition (2010)) (defining "chip select" as "a single line on a chip that will enable it to function when a signal is present"). Instead, as Netlist's own evidence shows, and as the plain language of "chip select" suggests, a chip select signal enables or selects a "corresponding" or "respective" array die. *See* '060 patent at 1:49-56 ("Each array die 110 also includes a chip select port 144, with the chip select ports 144 of the array dies 110 configured to receive ***corresponding*** chip select signals to enable or select the array dies for data transfer."); *id.* at 25:16-25 (reciting "chip select conduits for providing chip select signals to ***respective*** array dies") (emphasis added); *id.* at 24:31-36 ("control die further compris[ing] chip-select conduits, [and] . . . third die interconnects coupled between ***respective*** chip-select conduits and ***respective*** ones of the plurality of stacked array dies.") (emphasis added); *id.* at 25:28-30 ("wherein the chip select conduits include drivers to drive the chip select signals to the ***respective*** array dies") (emphasis added). Netlist's cited evidence is consistent with the rest of the description in the '060 and '160 patents, which routinely describes chip select signals in this manner rather than as enabling or selecting "one or more" array dies. *See, e.g.*, '060 patent at 10:57-60 ("Each of the chip select conduits 250 may be configured to provide a chip select signal to a ***corresponding*** array die 210 via a corresponding die interconnect 252.") (emphasis added); *id.* at 15:54-57 ("In some implementations, the drivers 404 a and 404 b

may drive a signal to the array die ***corresponding*** to the chip select signal, and not to array dies that do not correspond to a chip select signal.") (emphasis added).

Netlist's proposed construction is inconsistent with the stated goal of the '060 and '160 patents—to "reduc[e] the load of drivers of memory packages included on the memory modules," '060 patent at 1:19-21, because it would encompass the scenario where there is no reduction in load since all array dies are enabled at once. *See Terlep v. Brinkmann Corp.*, 418 F.3d 1379, 1382 (Fed. Cir. 2005) (rejecting construction that "would be inconsistent with the [] patent"); *see also Arbmetrics, LLC v. Dexcom Inc.*, 838 F. App'x 529, 533 (Fed. Cir. 2020) (rejecting a construction that is "plainly inconsistent with the purpose of the invention"); *KEYnetik, Inc. v. Samsung Elecs. Co.*, 837 F. App'x 786, 793 (Fed. Cir. 2020) (same). Indeed, Netlist's construction is inconsistent with the patents' only illustration of chip select conduits, interconnects, and signals: Figures 1A and 1B show one "chip select port" (items 144 and 174) per array die, and Figure 2 likewise shows one chip select conduit (item 250) and interconnect (252) per array die. *See, e.g., ERBE Elektromedizin GmbH v. Int'l Trade Comm'n*, 566 F.3d 1028, 1034 (Fed. Cir. 2009) (rejecting proposed construction that is inconsistent with the figures in the specification). Because Netlist cites no clear support for its unduly broad construction, and because Netlist's construction is inconsistent with the '060 and '160 patents' purpose and description of the invention, the Court should reject Netlist's proposed construction.

C. The '506 Patent

1. "before receiving the input C/A signals corresponding to the memory read operation"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
"during one or more previous memory operations"	the step of determining the first predetermined amount based at least on signals received by the first data buffer occurs before the earlier recited

	step of "receiving, at the module device, input C/A signals corresponding to a memory read operation via the C/A signal lines."[2]

Netlist does nothing more than restate the claim language in its proposal, but the intrinsic record supports Samsung's construction. According to the specification, the claimed "predetermined delay" is determined during a write operation, and is later used to time the transmission of a read operation – therefore claim 14's step of "determining the first predetermined amount" occurs "during one or more previous memory operations." *See, e.g.*, '506 patent at 4:9-19, 18:29-40, 18:49-64.

Netlist's amendments during prosecution further make clear that "before receiving the input C/A signals corresponding to the memory read operation" means "during one or more previous memory operations." After receiving a notice of allowance, Netlist amended nine claims by replacing the term "before the memory read operation" with "during one or more previous operations." *See* Ex. E at 2-8 (2020-10-16 Amendment After Notice of Allowance). By the applicant's own admission, these two terms were equivalent. *Id*. at 10 ("No new matter was added, and the amendment should not necessitate additional search or examination."). Indeed, applicants cannot change the scope of claims with an amendment after a notice of allowance. *See Genzyme Corp. v. Transkaryotic Therapies, Inc.*, 346 F.3d 1094, 1103-04 (Fed. Cir. 2003). Likewise, the term "before receiving the input C/A signals corresponding to the memory read operation" has the same scope as "before the memory read operation" because "receiving the input C/A signals corresponding to the memory read operation" is the first step of a memory read operation in the memory module – so, it simply means before a memory read operation. *See, e.g.*, '506 patent at 3:40-44. Given Netlist's interchangeable treatment of "before the memory read operation" and

[2] Netlist has construed the longer term: "[the method further comprising,] before receiving the input C/A signals corresponding to the memory read operation, determining the first predetermined amount based at least on signals received by the first data buffer"

"during one or more previous operations," the term "before receiving the input C/A signals corresponding to the memory read operation" also means "during one or more previous operations," and should be given the construction agreed to by the parties: "during one or more previous memory operations."

Netlist's sole reliance on *Virnetx* is flawed because the cannon of claim differentiation is merely a guide and cannot serve to broaden claims beyond their correct scope. *Curtiss-Wright Flow Control Corp. v. Velan, Inc.*, 438 F.3d 1374, 1381 (Fed. Cir. 2006). In *Virnetx,* the specification did not limit the claim term in question to the construction rejected by the court. *Virnetx, Inc. v. Cisco Sys., Inc.*, 767 F.3d 1308, 1317 (Fed. Cir. 2014). In contrast, ***all*** of the embodiments disclosed in the '506 patent specification perform the determining step during one or more previous memory operations. *See Curtiss-Wright*, 438 F.3d at 1380 ("[T]wo claims with different terminology can define the exact same subject matter.").

Without any explanation, Netlist states that any disclosure of the determination occurring during one or more previous memory operations is merely an embodiment. *See* Netlist Br. at 17. But in fact, the specification does not suggest any other embodiment where the determining step is ***not*** performed during a previous memory operation. *See Techtronic Indus. Co. v. Int'l Trade Comm'n*, 944 F.3d 901, 910 (Fed. Cir. 2019). Because of this and Netlist's amendments during prosecution, the Court should adopt Samsung's proposed construction.

D. The '339 Patent

1. "drive" claim terms

Representative Claim Term	Defendants' Proposed Construction	Plaintiff's Proposed Construction[3]
"each respective byte-wise buffer further includes	"each respective byte-wise buffer further includes logic configurable to, in	"time period in accordance with a

[3] Netlist's proposed construction of the limited phrase "time period in accordance with a latency parameter" is addressed in Section II.D.3 below.

logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter ***to actively drive*** a respective byte-wise section of the N-bit wide write data associated with the memory operation ***from the first side to the second side*** during the first time period" (claim 1)	response to the module control signals, ***activate*** *the byte-wise data path connected to a first DDR DRAM device* (in a first N-bit-wide rank), *and* ***disable*** *the byte-wise data path connected to a second DDR DRAM device* (in a second N-bit-wide rank), to cause a respective byte-wise section of the N-bit wide write data associated with the memory operation to be ***sent*** *from the first side to the first DDR DRAM device* ***along the activated*** *byte-wise data path and* ***not sent*** *to the second DDR DRAM device* ***along the disabled*** *byte-wise data path* during the first time period in accordance with a latency parameter."	latency parameter" means a time period wherein both the start of the time period and duration of the time period depends on at least a latency parameter. The remaining term requires no additional construction at this time (i.e., plain and ordinary meaning).

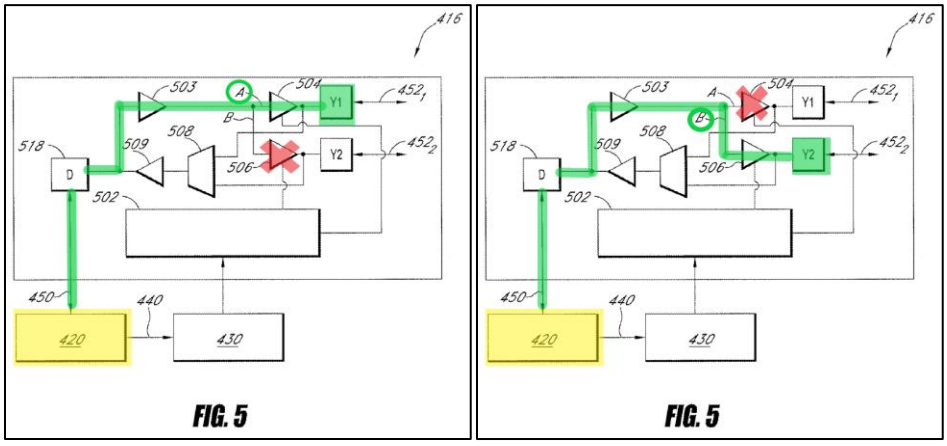
The independent claims of the '339 patent all recite a buffer or data transmission circuit with a "first side" coupled to the memory controller via "data signal lines" and a "second side" coupled to the DRAM devices via "module data lines." *See* '339 patent at claims 1, 11, 19, 27. Each of the six "drive" terms recites driving a section of data from the claimed "first side" (or the "data signal lines" coupled thereto) to the claimed "second side" (or the "module data lines" coupled thereto) for write operations, or from the "second side" to the "first side" for read operations. *Id.*; Dkt. 70-2, Exhibit B at 28-58. The claims make clear that "driving" data from one side of the buffer to the other side means ***activating one data path*** that is coupled to the memory device performing the memory operation (thus causing data to be sent to/from that memory device) and ***disabling other data paths*** that are not coupled to this memory device (thus causing data not to be sent to the memory devices coupled to these other data paths) – what Netlist characterizes as a "fork." *See* Netlist Br. at 2-4.

Figure 5, shown below, illustrates the "switching" described by the '339 specification. "[I]n a write operation, data entering a data transmission circuit 416 via a data line 518 is driven onto ***two data paths, labeled path A and path B***…The ranks of memory devices 412 are likewise

divided into two groups with one group associated with path A and one group associated with path B." '339 patent at 15:41-51 (emphasis added). For example:

> [W]hen the control logic circuitry 502 receives … an 'enable A' signal, a first tristate buffer 504 in path A is enabled and actively drives the data value on its output, while a second tristate buffer 506 in path B is disabled with its output in a high impedance condition… [and] … the data transmission circuit 416 allows the data to be directed along path A to a first terminal Y1, which is connected to and communicates only with the first group of the memory devices 412.… Similarly, if an 'enable B' signal is received, the first tristate 504 opens path A and the second tristate 506 closes path B, thus directing the data to a second terminal Y2, which is connected to and communicates only with the second group of the memory devices 412.

Id. at 16:12-25. Data paths A and B are similarly activated and disabled during read operations, depending on which memory device is performing the read. *Id*. at 16:26-36.



'339 patent at Fig. 5 (annotations added). The applicants confirmed this understanding during prosecution where they emphasized that the "fork" is what distinguishes their invention from the prior art: "[i]t is about controlling the data paths between the memory devices and the bus interface so that ***the data paths are open for a time period to allow data to be driven*** between the memory devices and the memory controller. This ***allows the data paths to be kept closed to isolate the memory devices*** from the bus interface when the memory module is not communicating data with the memory controller." Ex. F at 16 (2020-03-25 Amendment) (emphasis added); *see also* Ex. G at 14 (2020-06-24 Response); Ex. H at 21 (2020-07-24 Amendment). "Where an applicant argues

that a claim possesses a feature that the prior art does not possess in order to overcome a prior art rejection, the argument may serve to narrow the scope of otherwise broad claim language." *Seachange Intern., Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1372–73 (Fed. Cir. 2005).

The arguments made during prosecution confirm the alleged invention described in the specification. The '339 patent repeatedly describes the buffer (also referred to as a data transmission circuit) as a "switching circuit" and as "selectively allowing or inhibiting data transmission between the system memory controller 420, 420' and at least one selected memory device…" '339 patent at 8:41-47, 10:64-11:4, 11:35-12:14, 15:26-40.

There is no "straight-line" embodiment described in the '339 patent. In a desperate effort to engineer an infringement argument, Netlist ***fabricates*** figures that do not exist in the '339 patent. Netlist (at 4, 7) presents annotated versions of Figs. 4A and 4B of the '339 patent as examples of the "fork-in-the-road," which is what the '339 patent discloses. Netlist then claims that the "straight-line" layout is contemplated by the '339 patent by presenting ***altered versions of Figs. 4A and 4B with portions of the figures removed.*** *Id*. Netlist is forced to alter these figures because there is no figure in the '339 patent that discloses a straight-line layout (with only one data path). In fact, there is no disclosure or suggestion of a straight-line layout anywhere in the '339 patent.

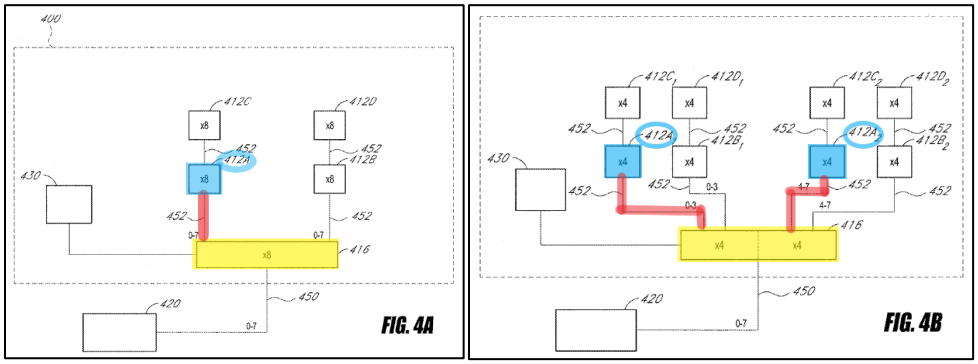
To accompany its fabricated figures, Netlist singles out <u>one word</u> in the entire '339 specification and claims that this single word contemplates a straight-line layout: "One or more of the data transmission circuits 416, in accordance with an embodiment of this disclosure, is operatively coupled to a corresponding ***one*** or more of the data lines 452 connected to one or more memory devices 412 in each of the ranks A, B, C, D." Netlist Br. at 7 (quoting '339 patent at 14:34-38) (emphasis in original). Netlist claims that the word "one" contemplates only one data path. But this passage is simply referring to the configurations shown in Figs. 4A and 4B – both of which require ***two*** separate data paths, and both of which correspond to Figure 5 – as made clear in the statements

that precede and follow the quoted passage. '339 patent at 14:15-34. The "one or more data lines" refers to the number of data lines used to connect to memory devices in a particular rank ("one or more of the data lines 452 connected to one or more memory devices 412 ***in each of the ranks A, B, C, D.***") *Id*. at 14:36-38 (emphasis added). It does ***not*** refer to the number of data paths used to transmit data to memory devices in different ranks.

For example, as shown below, in Fig. 4A, which Netlist concedes shows a "fork-in-the-road layout" with ***two*** data paths (Netlist Br. at 4), only one data line 452 is used to connect buffer 416 to a memory device in rank A (412A) since the buffer has the same bit width as the associated memory device (8 bits). *See* '339 patent at 13:43-48 ("The data transmission circuits of 416 of FIG. 4A has a bit width of 8 bits, and receives data bits 0-7 from the system memory controller 420 and selectively transmits the data bits 0-7 to selected memory devices 412A, 412B, 412C, 412D in response to the module control signals from the control circuit 430.").

In contrast, as seen in Fig. 4B below, which Netlist also concedes shows a "fork-in-the-road" layout with ***two*** data paths (Netlist Br. at 7), since the 8-bit width of buffer 416 is twice the 4-bit width of the memory devices, two data lines are used to connect buffer 416 to the memory devices in rank A ($412A_1$ and $412A_2$). *See* '339 patent at 14:1-8 ("The data transmission circuit 416 of FIG. 4B has a total bit width of 8 bits, and receives data bits 0-7 from the system memory controller 420 and selectively transmits data bits 0-3 to a first memory device $412A_1$, $412B_1$, $412C_1$, $412D_1$ and data bits 4-7 to a second memory device $412A_2$, $412B_2$, $412C_2$, $412D_2$ in response to the module control signals from the control circuit 430."). The configurations of Figs. 4A and 4B are shown in Figs. 3A and 3B as well – in Fig.3A, one data line connects the buffer to each rank, while in Fig.3B, two data lines connect the buffer to each rank. *Id*. at Figs. 3A, 3B. Thus, the number of data lines that connect the buffer to each rank does not change the fact that

the ’339 patent invention requires switching data paths between memory devices of different ranks depending on which memory device is performing the memory operation.



Id. at Figs. 4A, 4B (annotations added). In another attempt to force a straight-line configuration into the ’339 patent, Netlist argues that the benefit articulated in the specification of the memory controller only seeing a single load at each data buffer would also apply in a straight-line arrangement. Netlist Br. at 8 (quoting ’339 patent at 16:45-54). But Netlist omits the specification’s continued discussion of the reduced load as seen by the memory devices, which see a load from the multiplexor – and the multiplexor would not be necessary if there were no switching of data paths. ’339 patent at 16:53-64. In fact, the ’339 patent makes clear that the load reduction advantage is achieved by using the “fork” configuration:

> To reduce the memory device loads seen by the system memory controller 420 (e.g., during a write operation), the data transmission circuit 416 of certain embodiments is advantageously configured to be recognized by the system memory controller 420 as a single memory load. ***This advantageous result is desirably achieved in certain embodiments by using the data transmission circuits 416 to electrically couple only the enabled memory devices 412 to the memory controller 420*** (e.g., the one, two, or more memory devices 412 to which data is to be written) ***and to electrically isolate the other memory devices 412 from the memory controller 420*** (e.g., the one, two, or more memory devices 412 to which data is not written).

’339 patent at 14:59-15:4. In a further attempt to distance the ’339 patent from the “fork,” Netlist points to rulings in two prior ITC cases, involving a different defendant and two different patents related to the ’339 patent. First, according to Netlist, in ITC Inv. No. 337-ITC-1023 involving

U.S. Pat. No. 8,516,185, the ALJ limited the claims to a fork layout based on "selectively isolate" and "selectively allow" language in the claims. But this very same language is in the '339 patent specification when it describes the alleged invention, and the '339 patent applicants used equivalent language during prosecution in order to distinguish the '339 patent invention from the prior art, as explained above. Netlist also points to ITC Inv. No. 337-ITC-1089 involving U.S. Pat. No. 9,606,907 and argues that the ALJ in that investigation found that the fork configuration did not apply to those claims and deemed the claims infringed. But, this finding was not adopted by the Commission, which ultimately issued an order contrary to the ALJ's findings and found the claims not infringed. In any event, the prosecution history of the '339 patent carries more weight than extrinsic evidence related to different patents. *See Phillips v. AWH Corp.,* 415 F.3d 1303, 1317-18 (Fed. Cir. 2005). As explained above, the intrinsic record is clear that the "drive" claim terms ought to be given Samsung's proposed constructions.

2. "module controller" claim terms

Exemplary Claim Term	Defendants' Proposed Construction	Plaintiff's Proposed Construction
"a module controller . . . configurable to receive from the memory controller … input address and control signals for a memory write operation …, and to output registered address and control signals in response to receiving the input address and control signals…;"[4] (claim 1)	"a control circuit configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation … and corresponding to a number of ranks of memory devices lower than the physical number of ranks of memory devices on the module, and in response to receiving the input address and control signals, to output registered address and control signals corresponding to the number of physical ranks of memory devices on the module…"	No construction is necessary (i.e., plain and ordinary meaning).

[4] For simplification and clarity, Samsung presents only those portions of its proposed "module controller" claim terms and constructions that are in dispute.

The independent claims each include a "module controller" where the input signals correspond to a number of ranks of memory devices smaller than the actual (physical) number of ranks, which Netlist has described as rank multiplication. According to the '339 patent specification, the element corresponding to the claimed "module controller" is the "control circuit 430." '339 patent at 17:66-18:5. The specification states that "[e]xamples of circuits which can serve as the control circuit 430, 430' are described in more detail by U.S. Pat. Nos. 7,289,386 and 7,532,537, each of which is incorporated in its entirety by reference herein." *Id.* at 10:50-53. The control circuits disclosed in U.S. Pat. Nos. 7,289,386 (the "'386 patent") and 7,532,537 (the "'537 patent") are the ***only*** examples of control circuits provided by the '339 patent specification. *See id.* No other examples of control circuits are disclosed in the '339 patent.

Both the '386 and '537 patents disclose control circuits where the input signals correspond to a number of ranks of memory devices smaller than the physical number of ranks of memory devices. For example, the '386 patent discloses a control circuit where "the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices … are arranged, and the set of input control signals corresponds to a second number of ranks … for which the computer system is configured," and where "[t]he second number of ranks in certain embodiments is smaller than the first number of ranks." '386 patent at 7:6-14. The '537 patent also discloses a control circuit where "the set of output address and command signals corresponds to a first number of ranks in which the plurality of memory devices … are arranged, and the set of input address and command signals corresponds to a second number of ranks … for which the computer system is configured," and where "[t]he second number of ranks in certain embodiments is smaller than the first number of ranks." '537 patent at 16:19-26. Because the '339 patent's only disclosure regarding control circuits teaches that the input signals correspond to a number of ranks

of memory devices smaller than the actual number of ranks, it is clear that the claimed module controller must perform this function.

Netlist compares the claims of the ’339 and ’386 patents, but the claims of the ’386 patent are irrelevant to this case. What is relevant is the meaning of “module controller” as recited in the ’339 patent’s claims in light of what is disclosed in the specification. *See Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995), *aff'd*, 517 U.S. 370 (1996) (“Claims must be read in view of the specification, of which they are a part.”); *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1343 (Fed. Cir. 2001). Here, the claimed module controller is limited to a control circuit whose input signals correspond to a number of ranks of memory devices smaller than the actual number of ranks of memory devices because that is all that is described in the specification.

Netlist quotes the ’339 patent specification’s statement that “[t]he control circuit . . . registers signals from the control lines 440, 440' in a manner functionally comparable to the address register of a conventional RDIMM” as evidence that the ’339 patent contemplates a control circuit that does not perform what it describes as rank multiplication. *See* Netlist Br. at 10-11. But this portion of the specification merely refers to registering the input signals from the control lines. It says nothing about the control signals that are output from the control circuit.

Netlist claims that the so called rank multiplication is not needed in a two-rank memory module. Netlist Br. at 11. But the ’386 patent in fact discloses an example of a two-rank memory module with a control circuit where the input signals correspond to a number of memory devices smaller than the actual number of memory devices. *See* ’386 patent at Fig. 1B, 7:16-18.

As Netlist acknowledges, excluding a preferred embodiment is rarely if ever correct. *Kaufman v. Microsoft Corp.*, 34 F.4th 1360, 1372 (Fed. Cir. 2022). A control circuit where the input signals correspond to a number of ranks of memory devices smaller than the actual number

of ranks of memory devices is the ***only*** embodiment disclosed and contemplated by the '339 patent. Therefore, it cannot be excluded from the construction of the "module controller" term. *See, e.g.*, *Techtronic*, 944 F.3d at 910; *Cortland Line Co., Inc. v. Orvis Co., Inc.*, 203 F.3d 1351, 1357 (Fed. Cir. 2000) (limiting the claim term "means for connecting said second end plate to said first spool axle" to being a threaded connector or structural equivalents thereof because a threaded connector was the only embodiment of the connecting means described in the specification); *Netcraft Corp. v. eBay, Inc.*, 549 F.3d 1394, 1397–1400 (Fed. Cir. 2008). Thus, the Court should adopt Samsung's construction because the '339 patent's specification only discloses embodiments of module controllers where the input signals correspond to a number of ranks of memory devices smaller than the actual number of ranks of memory devices, which Netlist describes as rank multiplication.

3. "latency parameter" claim terms

Claim Term	Defendants' Proposed Construction	Plaintiff's Proposed Construction
"time period in accordance with a latency parameter" '339, claims 1, 11, 34, 35	Plain and ordinary meaning.	"a time period wherein both the start of the time period and duration of the time period depends on at least a latency parameter"

Netlist attempts to create a limitation ("duration") that has no support in the specification. In fact, Netlist's proposed construction of "time period in accordance with a latency parameter" contradicts the specification itself, which states that the "latency parameter" "is known" as "a delay time" which indicates "the ***moment*** the data . . . is on the output pins." '339 patent at 15:61–16:6 (emphasis added). Thus, the "latency" is simply the amount by which the start of a data transfer is delayed. There is no support for Netlist's argument that the "latency" determines the ***duration*** of a data transfer as well. Figure 6, referenced by Netlist, shows only generic time periods (e.g., time periods 601, 602, 603, etc.) and neither the figure nor the corresponding description articulate the details of how the latency parameter relates to these time periods. There is certainly no

reference to the latency parameter affecting the ***duration*** of how long the data is driven. Likewise, Netlist's reliance on the language that "[r]ecalling the CAS latency described above, each write operation extends over two time periods in a pipelined manner" simply references latency with respect to the "pipelined manner" in which the write operations happen, not the duration of the operations. '339 patent at 17:63-65.

Contrary to Netlist's arguments, the '339 patent does not disclose any details of how "latency" should be taken into account, leaving it for one of ordinary skill to figure out. The specification concedes that the CAS latency is known in the art. '339 patent at 15:61-66 ("As is known, Column Address Strobe (CAS) latency…"). And, during prosecution, similar claim language ("specific time period") was found obvious by the Examiner in view of the JEDEC standards, which define all the relevant timing considerations, thus making it clear that one or ordinary skill in the art would understand the timing and latency aspects of the '339 patent. *See, e.g.*, Ex. I at 11 (2019-10-03 Non-Final Rejection) ("One of ordinary skill in the art at the time of the invention would be aware of the JEDEC Standard 21-C for DDR SDRAM Registered DIMM which includes timing information (for example page 67 shows specific timing information)."); Ex. J at 9 (2020-04-24 Final Rejection). Given the above, the plain and ordinary meaning of the claim language sufficiently defines the claimed "time period in accordance with a latency parameter" and no further construction is necessary, especially not one completely unsupported by the intrinsic evidence.

CONCLUSION

For the reasons recited above, Samsung requests that the Court adopt Samsung's proposed claim constructions.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the foregoing document was filed electronically in compliance with Local Rule CV-5 on September 16, 2022. As of this date, all counsel of record have consented to electronic service and are being served with a copy of this document through the Court's CM/ECF system under Local Rule CV-5(a)(3)(A).

/s/ Francis J. Albert